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10/644,718	08/20/2003	Yi-Hsun Wu	N1085-00191	6119

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EXAMINER	
NGUYEN, DANNY	
ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/644,718	WU ET AL.	
	Examiner	Art Unit	
	Danny Nguyen	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,12-21 and 23-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,12,13,15-21,23-28* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/21/2007 have been fully considered. Regarding the arguments of claim 1 is found not persuasive and. And regarding the arguments with respect to claims 7, 13 and 23 are found persuasive and moot in view of new ground of rejection.

Regarding claim 1, applicant argued that Lien does not disclose the device coupled to the voltage drop comprises an NMOS transistor. Examiner respectfully disagrees with the arguments. Line does disclose the device (121) coupled to the voltage drop (122-1-1125) comprises an NMOS transistor (NMOS transistor 121, see col. 7, line 5-6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim Rejections - 35 USC § 102

2. Claims 1-4, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien et al (USPN 6,069,782) in view of Smith et al (USPN 6,775,112).

Regarding claim 1, Lien discloses a sensor (125 in figure 2b) for electrostatic discharge protection comprises an inverter (such as 123) coupled to the output terminal (126) of the sensor, a voltage drop circuit (series diodes 122-1 to 122-5) coupled to an

input terminal (101) of the sensor, wherein a voltage drop occurs across the voltage drop circuit and a high state voltage is generated at an output terminal (126) of the sensor when the input terminal of the sensor is coupled to an ESD voltage pulse (ESD voltage pulse on terminal 101), thereby, applying the high state voltage to the inverter, and a device (such as 121) coupled to the voltage drop circuit, wherein the device is adapted to maintain the high state voltage at the output terminal of the sensor, while the input terminal of the sensor is coupled to the ESD voltage pulse, wherein the device comprise a NMOS transistor (see col. 7, lines 5-6), wherein the output terminal of the inverter is coupled to a gate terminal of an ESD protection circuit (124) (col. 7, lines 5-59). Lien does not disclose the cascaded transistor as claimed. Smith discloses an ESD circuit comprises a MOS transistor of ESD circuit is cascaded NMOS (300) (figures 3 and 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ESD circuit of Lien to incorporate the cascaded transistor as disclosed by Smith in order to provide efficient ESD protection.

Regarding claim 2, Lien discloses the input terminal of the sensor is coupled to a voltage supply terminal (101).

Regarding claims 3, 4, Lien discloses the voltage drop circuit is a series of diodes (122-1 to 122-5).

Regarding claim 12, Lien discloses the gate of the MOS transistor (124) is pulled down to a low state when the ESD pulse is sensed (col. 7, lines 5-53).

3. Claims 13, 15-20, 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien et al (USPN 6,069,782) in view of Stockinger et al (USPN 6,970,336).

Regarding claim 13, Lien discloses a circuit (figure 2b) for ESD protection comprises an ESD circuit having a MOS transistor (124) with a gate terminal, wherein the transistor is configured to discharge an ESD pulse, a sensor (125) that senses an ESD pulse and generates a high state voltage at an output terminal in response to the ESD pulse, and an inverter (such as inverter 123) coupled to the output terminal of the sensor and the ESD circuit, wherein the sensor applied the high state voltage to an input terminal of the inverter (see col. 7, lines 5-53). Lien does not disclose the stack of cascaded transistor as claimed. Stockinger discloses an ESD circuit (figure 4) comprises an ESD protection circuit configured to discharge an ESD pulse having a tack of cascaded NMOS transistors (a stack of cascaded NMOS transistors 407, 409, 425, 427 of the shunting circuit 405, 423). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ESD circuit of Lien to incorporate the stack of cascaded transistors as disclosed by Stockinger in order to improve t ESD protection (col. 3, lines 1-4).

Regarding claims 15, 16, Lien discloses the sensor (125) for electrostatic discharge protection comprises a voltage drop circuit (series diodes 122-1 to122-5) coupled to an input terminal (101) of the sensor, wherein a voltage drop occurs across the voltage drop circuit and the high state voltage is generated at an output terminal (126) of the sensor when the input terminal of the sensor is coupled to an ESD voltage

pulse (ESD voltage pulse on terminal 101), and a device (such as 121) coupled to the voltage drop circuit, wherein the device is adapted to maintain the high state voltage at the output terminal of the sensor, while the input terminal of the sensor is coupled to the ESD voltage pulse (col. 7, lines 5-53).

Regarding claims 17, and 18, Lien discloses the voltage drop circuit is a series of diodes (122-1 to 122-5).

Regarding claims 19, 20, Lien discloses the device comprises a NMOS transistor (121) (see col. 7, lines 5-6).

Regarding claims 23, 24, 27, Lien discloses a method for ESD protection comprises sensing an ESD pulse (the ESD pulse is sensed by circuit 125), pulling down a gate terminal of a MOS transistor (124) of an ESD circuit to a low state when the ESD pulse is sensed, wherein the transistor is configured to discharge the ESD pulse (as the ESD is detected, the transistor 222 turn on to pull the gate of the transistor 124 to a low state voltage (col. 7, lines 5-53). Lien does not disclose stack of cascaded transistors as claimed. Stockinger discloses an ESD circuit (figure 4) comprises an ESD protection circuit configured to discharge an ESD pulse having a tack of cascaded NMOS transistors (a stack of cascaded NMOS transistors 407, 409, 425, 427 of the shunting circuit 405, 423). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ESD circuit of Lien to incorporate the stack of cascaded transistors as disclosed by Stockinger in order to improve t ESD protection (col. 3, lines 1-4).

Regarding claims 25, 26 Lien discloses connecting the sensor to a voltage supply terminal (Vcc) and generating a high state voltage at the output terminal when the ESD pulse is sensed.

Regarding claim 28 Lien discloses connecting the output terminal of the inverter (123) to the input of the ESD protection circuit (124).

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lien et al (USPN 6,069,782) in view of Smith et al (USPN 6,775,112), and Dungan et al (USPN 5,311,391). Lien and Smith disclose all limitations of claim 1 as discussed above, but do not disclose a gate and a drain of the NMOS transistor as claimed. Dungan discloses an ESD protection circuit (figure 2) comprises a gate and a drain of a NMOS transistor (NMOS transistor 51f) are common and coupled to the output (53) of a sensor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device of Lien and Smith to incorporate the NMOS transistor as disclosed by Dungan in order to minimize leakage in the circuit (col. 1, lines 65-68).

5. Claims 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Lien et al (USPN 6,069,782) in view of Stockinger et al (USPN 6,970,336), and Dungan et al (USPN 5,311,391). Lien and Stockinger disclose all limitations of claim 13 as discussed above, but do not disclose a gate and a drain of the NMOS transistor as claimed. Dungan discloses an ESD protection circuit (figure 2) comprises a gate and a drain of a NMOS transistor (NMOS transistor 51f) are common. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the

device of Lien and Stockinger to incorporate the NMOS transistor as disclosed by Dungan in order to minimize leakage in the circuit (col. 1, lines 65-68).

Allowable Subject Matter

6. Claim14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is 571-272-2054. The examiner can normally be reached on 8:00-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MICHAEL SHERRY can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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10/15/2007

10/28/07

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER